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Infineon Single Chip Solution for IP-Phone Applications

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Preliminary Hardware Design Guide

Revision 1.

Communication Solutions



Never stop thinking

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Table of Contents

Table of Contents

1	Conception of the Phone		8
1.1	Choice of Components		8
1.1.1	Crystal versus Oscillator		8
1.1.2	DDR-SRAM versus SDR-SDRAM		8
1.1.3	Choice of Flash		8
1.1.4	Power-Supply Selection		8
1.1.5	Selection of External Phy		9
1.1.6	Selection of Loudspeaker		9
1.1.7	Selection of Microphone		9
1.1.8	Selection of Display	1	0
1.1.9	Annotation to ESD-protections	1	0
1.1.10	Annotation to the Power-Sequence		
1.2	Connections to the Periphery of the INCA-IP2		
1.2.1	PCM-Interface		
1.2.2	SSC0-Interface		
1.2.3	SSC1-Interface		
1.2.4	External Bus Unit		
1.2.5	Keypad Scanner		
1.2.6	LED-Control		
1.2.7	ASC0 Interface		
1.2.8	Ethernet Interfaces		
1.2.9	Analogue Frontend		
1.2.10	Interrupt-Pins		
1.2.11	NMI-Interrupt-Pin		
1.3	Hints for a Sophisticated Design		
1.3.1	PCB-Detection		
1.3.2	Free interfaces		
2	Schematic Design Guide		
_			
2.1	Boot-Strapping of the INCA-IP2		
2.2	Oscillator Interface XTAL1 and XTAL2		
2.3	Debug Interfaces		
2.3.1	Test Clocks		
2.3.2	Phy Test Pins		
2.3.3	JTAG Interface		
2.3.4	EJTAG-Interface		
2.4	Reset Circuitry		
2.5	Connection to Flash		
2.5.1	NOR-Based Flash		
2.5.2	NAND-Based Flash		-
2.5.3	SPI-Flash		
2.6	Volatile Memory		
2.6.1	Connection to SDR-SDRAM		
2.6.2	Connection to DDR-SDRAM		
2.7	Ethernet Interface		
2.7.1	Gigabit Ethernet		
2.7.2	Internal 10/100-Phys		
2.8	ASC0 Terminal Interface		
2.9	Analogue Frontend	1	9



CONFIDENTIAL

Table of Contents

4	Layout Study	35
3.13	Checklist for Layout-Release	33
3.12	Hints to be realized in Software	33
3.11	USB-Layout	33
3.10	Layout of ASC0	33
3.9	Layout of the AFE	32
3.8.2	Layout of external Phys	31
3.8.1	Layout of the Internal Phy	31
3.8	Layout of the Ethernet Interfaces	31
3.7.5	Final Annotations to DDR-SDRAM Layout	
3.7.4	Additional Layout Rules	
3.7.3	Layout Rules against unequal Signal Propagation	
3.7.2	Layout Rules against Cross Talk	
3.7.1	Layout Rules against Reflections	28
3.7	DDR-SDRAM	
3.6	SDR-SDRAM Layout	28
3.5	Layout of the Crystal or Oscillator	27
3.4	Layer Stack Setup	27
3.3	Execution of the Power-Plane	26
3.2	Execution of the GND-Plane	26
3.1	General Layout-Hints	24
3	Layout	24
2.12	Checklist for Schematic Release	22
2.11	LED-Circuitries	21
2.10	Circuitry for Keypad	20
2.9.3	Circuitries for Loudspeaker	20
2.9.2	Circuitry for Earpiece Output	19
2.9.1	Circuitry for Microphones	19



List of Figures

List of Figures

Figure 1	Overview of the Pin-multiplexing of the INCA-IP2	11
Figure 2	Oscillator Interface with Crystal	15
Figure 3	Circuitry to Delay Power On Reset.	16
Figure 4	How to Connect SDRAM-Modules	17
Figure 5	External Circuitry of the Internal Phy	18
Figure 6	Microphone Circuitry for INCA-IP2	19
Figure 7	Loudspeaker Circuitry of the INCA-IP2.	20
Figure 8	Example for Full Matrix Mode Keyboard.	21
Figure 9	Circuitries for LED-connections	22
Figure 10	Placing Block Capacitor to Reduce EMI	24
Figure 11	Arrangement of Vias under a BGA	25
Figure 12	Arrangement of vVias of a Data-bus.	26
Figure 13	Ideas for Power-planes.	27
Figure 14	Layout of Crystal.	28
Figure 15	Top View on RGMII CLKs.	31
Figure 16	Elevation of RGMII CLKs	32
Figure 17	Layout Study for DDR-RAM Connection to P-TSOP2	35
Figure 18	Layout Study for the RGMII-Interface	36
Figure 19	Layout Study for the EBU-balls, Key-signals, JTAG-interface and LED-signals	37



List of Tables

List of Tables

Table 1	Boot Sources (devices to boot from)	14
Table 2	Internal Length of DDR-SDRAM Signals (BGA-324 Package)	29



Conception of the Phone

1 Conception of the Phone

The INCA-IP2 can be used for low-cost phones as well as for high end phones. To achieve this a very flexible architecture is used. The balls of the INCA-IP2 are multiplexed in many cases and many interfaces are available.

This chapter intends to provide you an overview of possibilities. The details are discussed in Chapter 2.

1.1 Choice of Components

1.1.1 Crystal versus Oscillator

You can use the INCA-IP2 with an Oscillator, but there is no reason to avoid the use of the cheaper Crystal. If there are several devices on the board which can use the same clock source, the INCA-IP2 can run in oscillator-mode.

It is also possible to use one of the two clock outputs of the INCA-IP2 to provide the signal to the periphery. In this case the jitter and the signal-quality must be double-checked in detail. If the clock signal runs through an internal PLL of the INCA-IP2 an additional jitter is introduced.

1.1.2 DDR-SRAM versus SDR-SDRAM

The main reason to provide two kind of RAMs is the unpredictability of pricing. The INCA-IP2 preforms excellently with both kind of volatile storages, whereas the use of DDR-SDRAM still increases the speed of the system.

The delivered Phone Application software, which is good for an enhanced graphical wide-band-phone needs less than 16 MByte SDRAM. The Linux OS is runs on SDRAM completely.

Low-cost-phones can also work with less memory, but additional software-effort may be needed.

To calculate the real costs, the additional 2.5 V power-supply for the DDR-SDRAM must be taken into account. This power-supply can be used for other devices too. The 2.5 V supply can be very low cost.

There is little software effort needed to switch from SDR-SDRAM to DDR-SDRAM or vice versa. To make a combo design with both RAM-types is not recommended.

1.1.3 Choice of Flash

Serial and parallel NOR-based flash can be used as well as NAND-based flash. The NOR-based flash is more expensive and slower than NAND-based flash. The NOR-based devices can work with an 8 or 16 bit wide bus. NAND-based flash is only available in bigger modules so that it is not cheap enough for low-cost phones. In former times the data integrity of NAND-based flash was a problem, and it should be double-checked today, too. The long time availability should be clarified with the supplier.

Note: The use of serial flash instead of a parallel flash makes it easier to develop a four-layer design.

1.1.4 **Power-Supply Selection**

The INCA-IP2 needs a 1.5 V and a 3.3 V power supply. If a DDR-RAM is used, there is also a 2.5 V needed.

The expected maximum consumption of the INCA-IP2 is less than 600 mA for 1.5 V. The theoretical transient consumption can be higher and so a reserve of 300 mA should be provided for the INCA-IP2¹).

Using two 64 MByte devices the highest maximum consumption in a realistic scenario is less than 150mA for the 2.5 V power supply. This includes the two DDR-RAM modules and the INCA-IP2. The theoretical transient consumption can be up to 300 mA.

¹⁾ The absolute peak consumption is measured with programs which are far away from a reasonable application, but only to stress the chip.



Conception of the Phone

The 3.3 V power consumption is significantly lower using DDR-SDRAM memory. The dimensioning of the 3,. V power supply is more dependent of the periphery.

The heat dissipation should be limited by using the sophisticated power management features of the INCA-IP2.

There are no special needs to a Power-over-Ethernet-supply. If the power is switched down to 3.3 V directly, the power-sequence of the INCA-IP2 must be taken into account. It is important that the 1.5 V must be available first. For more details look at **Chapter 1.1.10**.

The necessity of the galvanic separation of the PoE-supply should be discussed according the features of the phone. If the USB-interface, a second Ethernet-port or a power-plug is available outside the housing, a separation should always be used. In this cases the remote power-supply could easily run into problems without a galvanic separation. You can find more details in the IEEE 802.3af specification.

1.1.5 Selection of External Phy

You can find several GbE Phys in the market which work together with the INCA-IP2. The Phy must have an RGMII-interface and a small power-consumption to prevent the need of a fan. Some Phys can work with 2.5 V on the RGMII. If those input-pins are 3.3 V tolerant they may work with the INCA-IP2 without level shifter. In chapter 32.3 of the User's Manual Hardware Description you can find details for the needed input levels.

In case of using PoE it might be cheaper to use one transformer for each port, as a PoE transformer can be more expensive.

It is not possible to use an internal and an external phy at the same time.

1.1.6 Selection of Loudspeaker

The INCA-IP2 provides an internal amplifier for one Loudspeaker. This amplifier may not provide sufficient output power for high volume scenarios or may not fit to the impedance of the selected loudspeaker. The INCA-IP2 Reference-System provides the possibility to compare the sound of an external class-d amplifier and the internal amplifier of the INCA-IP2. So It is easy to find the right choice for every phone.

For a good performance the Loudspeaker should have the following features:

- The frequency response should be well-balanced and linear.
- The frequency responses should support good responses for 300 Hz to 3.4 kHz for narrowband and 150 Hz to 6.3 kHz for wideband applications.
- The impedance of the speaker should be around 25 Ohms. Impedances down to 20 Ohms are no risk for the INCA-IP2. Impedance like 8 Ohms must not be used, as the lifetime can not be predicted. External amplifier may support other impedances.
- The Total Harmonic Distortion (THD) should be smaller than 5%.
- The volume behind the loudspeaker should be as big as possible.
- The chamber behind the loudspeaker should be shut as tightly as possible.

There are following indications for a good loudspeaker:

- The bigger the diameter of the loudspeaker the better the sound. A diameter of less than 50 mm is critical.
- A metal housing is preferred.
- A double suspension helps normally for a linear movement

1.1.7 Selection of Microphone

For a good performance the following hints should be used:

- A good signal-to-noise Ratio (>64 dB is recommended) is helpful for good results. Micros with a diameter around 10 mm or more have normally good SNR.
- The microphone connection should be balanced.
- The microphones must be unidirectional and the mounting must prevent acoustic influences from inside the phone.



CONFIDENTIAL

Conception of the Phone

- The microphone must have a mechanical decoupling from the housing to protect against structure-borne sound.
- The bias-voltage of the microphone must fit to the provided filter (see Figure 6) and should not exceed 3 V.

1.1.8 Selection of Display

Displays or display-controller are either connected to the External Bus Unit (EBU) or to one of the SPI-Interfaces. Normally the SPI-Interface is the best interface to send the data to the display. The SPI-Interface of the INCA-IP2 is provided with Direct Memory Access (DMA), which cares for a fast interface without much performance loss of the CPU. The System is easier to layout and EMI-limitations are less significant. The INCA-IP2 Reference System shows a solution with a WQVGA-color display connected to the SPI interface.

The EBU is the right choice if a VGA-color-display is used. In this case a big amount of data must be sent in a fractional of a second. Most of the graphic controller do not have an SPI-Interface which is fast enough to receive such an amount of data fast enough.

Of course the EBU can also be used if there are other reasons to use a special display.

1.1.9 Annotation to ESD-protections

The INCA-IP2 has an on-chip ESD-protection which is qualified according to the Human Body Model (HBM) and the Charge Device Model CDM ¹⁾. The qualification is made to meet PCB-production purposes. So it is not risk-free to omit additional ESD-protections on the interfaces, which are used by the end-customer.

The use of additional ESD-protections is dependent of the used interfaces, the circumstances on the board and the target market. In general you can seldom find ESD-protections on Ethernet and USB-Interfaces which does not mean that any risk is excluded. An ESD-protection on the headset/handset is much more common. Especially the headset is often plugged by the end-customer and therefore more endangered.

1.1.10 Annotation to the Power-Sequence

The power-sequence can cause significant costs. Microcontrollers normally need the core-voltage first. The core voltage is needed to control the pads. If the voltage for the pads would be available first, it could happen that the MOSFET which has to pull the signal up and the MOSFET which has to pull the signal down are open at the same time. As a result there would be a big cross current. Some Microcontrollers stay in a latch up condition after those currents.

The INCA-IP2 can stand currents below 100 mA for some nano seconds. This would mean that a simultaneous power-up of 1,5.V and 3.3 V is possible.

These are the rules for the power-sequence of the INCA-IP2:

- The 1.5 V supply must ramp up simultaneously or earlier than the 3.3 V supply.
- There is no maximum-delay between the 1.5 V and 3.3 V and the 2.5 V supply.
- All 3.3 V supplies must ramp up simultaneously.
- The sequence of the ramp up of 2.5 V correlated to 3.3 V is irrelevant.
- There is no needed power down sequence.

The power-sequences of other controllers/phys and so on must be taken into account.

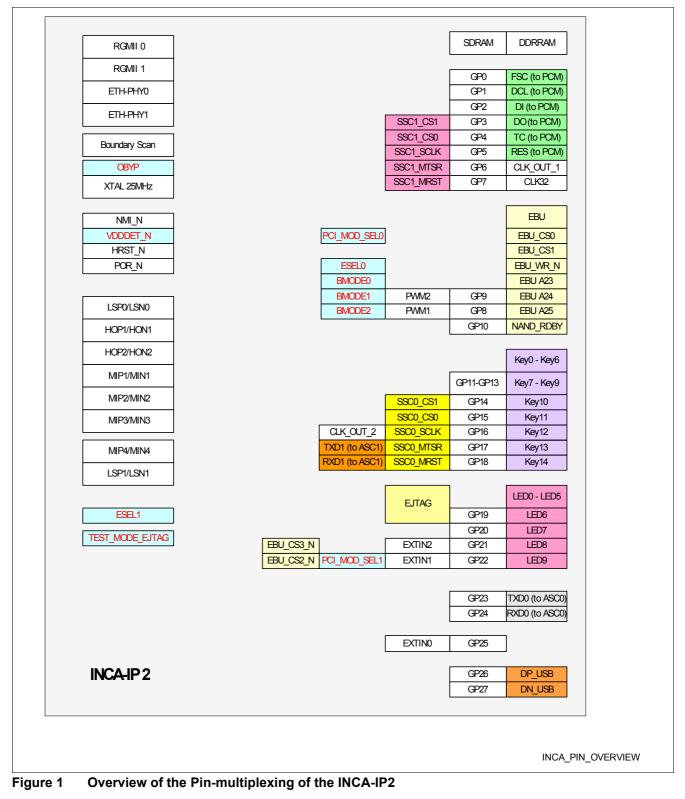
1.2 Connections to the Periphery of the INCA-IP2

This chapter gives an overview how to select the appropriate interfaces for the target application and to overcome pitfalls. After having an idea of the used components it is important to connect it correctly and to find an optimized interface arrangement.

¹⁾ For more details look at the User's Manual Hardware Description.



Conception of the Phone



In **Figure 1** there is an overview of the pins of the INCA-IP2. On the left side you can see the not multiplexed pins. On the right side there are the multiplexed pins shown. The possible pin meanings are shown in one row for each pin or group of pins. Every shown pin can be adjusted separately. The signals are grouped to make a sensible use more obvious but the groups are not reasoned by limitations.

In the following paragraphs you will find hints for each interface.



Conception of the Phone

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1.2.1 PCM-Interface

In **Figure 1** you can see the PCM-Interface-Pins marked in green. If you decide to use a PCM-Interface not necessarily all pins of this interface must be used, as every pin is characterized separately. In most applications the TC-pin and the RES-pin are used as General Purpose Pin or as a part of the SSC-Interface.

1.2.2 SSC0-Interface

The SSC0/SPI0-Interface (marked in yellow) is partly multiplexed with the keyscanner-interface. If there are more than 66 keys needed this interface can not be used.

1.2.3 SSC1-Interface

The SSC1/SPI1-Interface (marked in light-red) is partly multiplexed with the PCM-Interface, but this is normally no problem. Every GP-Pin can serve as a Chip-Select for the SSC-Interface if more than one is needed. Do not use the SSC1-Interface for a Flash, if you intend to boot from it. It is only possible to boot from SPI0-Interface.

1.2.4 External Bus Unit

It is possible to connect a NAND-based flash to the EBU (marked in light yellow) and to use it also for other applications which use a parallel bus. There is no big software effort needed for this. The highest address bits can be used for other purposes, as such a big address range is seldom needed.

If a parallel NOR-based flash is used for booting, the CS0 must be used to address the flash. After reset or powerup, the NOR-based Flash must be ready before the INCA-IP2 starts its first code-fetch.

1.2.5 Keypad Scanner

The Keypad Scanner (marked in violet) can detect more than one key press at the same time, but not all key combinations are possible. If you use a not allowed combination it will not disturb the system, but a key-press might be lost. If designed properly, the Keypad Scanner can also be used for the Hook-Switch or for multiplexed meanings of function keys for example.

The Keypad-Scanner is interrupt controlled. So you can generate an interrupt-driven Hook-Switch without using one of the Interrupt-Pins.

1.2.6 LED-Control

If you want to control an LED, you can simply use a General Purpose Pin for this. The LED-matrix (marked in light red) allows to control up to 24 LEDs with only 10 pins. Blue or white LEDs normally need a higher forward voltage and may have loss in brightness if you do not use an appropriate circuitry.

1.2.7 ASC0 Interface

The ASC0 interface (marked in grey) is a very helpful interface to develop software and debug the board. If this interface is used in the system for other purposed too, it should be available for debug purposes alternatively. The Reference System of the INCA-IP2 gives an example for this. In principle it is possible to debug via ASC1 interface too, but if you want to boot via a UART interface, than you need the ASC0.

1.2.8 Ethernet Interfaces

The Ethernet Interfaces are not multiplexed and you can develop a PCB with a mounting option for an external GbE Phy.



Schematic Design Guide

1.2.9 Analogue Frontend

The MIP/MIN, HOP/HON, LSP/LSN signal should be used similar to the INCA-IP2 Reference System. This approach ensures an easy alignment of firmware improvements.

Details of the circuitry may differ in accordance to cost-reduction or hardware alignment to speaker and micro.

The two input-signals of not used microphones should be shortened.

1.2.10 Interrupt-Pins

The INCA-IP2 provides three external Interrupt signals. On the EXIN1 interrupt pin there must be a resistor for boot-strapping¹⁾. In most of the cases this resistor is a pull-down (see **Chapter 2.1**). As a result this Interrupt pin is not feasible to connect Interrupt outputs which need a pull-up.

1.2.11 NMI-Interrupt-Pin

The NMI must not be used as a normal interrupt. Normally it is simply connected to 3,3V. For details refer to the User's Manual Hardware Description.

1.3 Hints for a Sophisticated Design

1.3.1 PCB-Detection

In **Figure 1** you can see the Pin multiplexing of the INCA-IP2. The configuration of a pin can not change in Linux but there might be a different configuration in u-boot and Linux operation. This offers the possibility to read the status from a pin while starting with the u-boot, which is later used as an output. So you can identify a PCB and adjust the software accordingly. For example you can give every PCB-version another identification to react on hardware-changes, or you can mark placing-options.

1.3.2 Free interfaces

The INCA-IP2 gives multiple chances to reduce the needed pins. Here it may be helpful to limit the needed interfaces to have them available for later used applications.

2 Schematic Design Guide

The Schematics of the INCA-IP2 Reference System are helpful to get a fast and good example. The Bill of Material of the Reference-System is not minimized. You may reduce costs by removing features or reducing quality. In the following paragraphs the circuitry around the INCA-IP2 is described from the center to the periphery.

2.1 Boot-Strapping of the INCA-IP2

Most of the settings of the INCA-IP2 can be programmed, but some choices have to be clear at startup. This Boot-Strap-Signals are marked in light blue in **Figure 1**.

There are six variable features which must be clear at startup:

- The device to boot from
- The mode of the parallel interface
- The endianess of the CPUs
- The choice of the CLK-source
- The usage of the internal undervoltage detection

¹⁾ A boot-strap pin defines several modes of the Chip before it starts to boot



- The usage of the EJTAG-Interface
- In **Table 1** you can see the needed settings for each possible boot device:

BMODE(2:0)	Boot Source	Remark
000	EBU (NOR-based flash)	
001	ASC0	115 baud, 8 bit, no parity, 1 stop-bit, no flow control
010	SPI0 (generic)	Vendors like ST or others
011	SPI0 (ATMEL)	Boot with ATMEL command set
100	EBU NAND (small page)	For 528 byte (small page NAND)
101	EBU NAND (large page)	For 2112 byte (large page NAND)
110	Reserved	Reserved
111	Debug	Boot modi via terminal adjusted

Table 1 Boot Sources (devices to boot from)

The Boot-Strap-Signals BMODE0 to BMODE2 must be set to 3.3 V or GND according to Table 1.

The parallel interface can be used for PCI applications or as a generic EBU. For the INCA-IP2 only the EBU is supported and for this the PCI_MOD_SEL0 and PCI_MOD_SEL1 signal must be set to GND.

The Endianess of the two CPUs must be set according to the used operating system. The firmware on CPU1 is using big endian and so ESEL1 must be set to 3.3 V. If Linux is used the CPU0 must always be big endian. In this case ESEL0 must also be set to 3.3 V. If other operating systems than Linux are used the endianess must be advised by the responsible software engineers.

As described in **Chapter 1.1.1** most likely a crystal is used. For using a crystal the OBYP-signal must be set to GND. If you do this directly without a pull-down, this can ease the work of the layouter.

The internal undervoltage detection-level is set to not very sensitive levels. As a result you can enable it, even if you use an external reset-device too. To enable the undervoltage detection VDDDET it must be set to GND.

In the normal operating-mode the EJTAG-mode should be disabled. For this the TEST_MODE_EJTAG signal must be set to GND via a resistor.

The pin-strapping can be designed by connecting the signals via resistors to 3.3 V or GND. In case of not multiplexed signals like OBYP, VDDDET, ESEL1, the signal can be put go GND or 3.3 V directly. For Signals which are multiplexed like the BMODE and PCI_MOD_SEL, values between 10 kOhm and 20 kOhm are used in common.

It is strongly recommended to strap the TEST_MODE_EJTAG pin with a resistor. Otherwise you inhibit the testmode if needed.

For debug purposes it may help to enable the easy boot via ASC. At the INCA-IP2 Reference System for example there are openings in the housing and landing-pads on the PCB to make a boot via ASC possible without opening the housing. Therefore diagnostics are possible much easier.

2.2 Oscillator Interface XTAL1 and XTAL2

A crystal should be connected as shown in **Figure 2**. The two resistors need not be used. They are implemented for fall back solutions but were not used up to the date of writing the Design Guide. In case of having an unusual crystal this resistors may help.



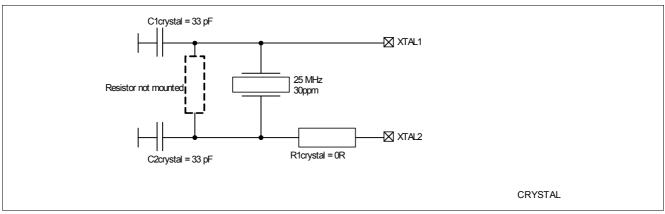


Figure 2 Oscillator Interface with Crystal

You can find the detailed Crystal specification in chapter 32.4.3 of the User's Manual Hardware Description.

If an oscillator is used instead of a crystal, there is no special circuitry necessary. For noise-reduction you can precautionary place a not mounted 33 pF capacitor between the XTAL1-pin and GND.

2.3 Debug Interfaces

2.3.1 Test Clocks

The Test Clocks TESTCLK1, TESTCLK2, TESTCLK3, TESTCLK4 and TEST_MODE_CLK are for Infineon test purposes only. They should be connected to GND directly.

2.3.2 Phy Test Pins

The 10/100 Ethernet Phy of the INCA-IP2 has two test-pins. They are for Infineon test purposes only. They should be directly connected to GND without any resister to ease the Layout.

2.3.3 JTAG Interface

The JTAG Interface consists of the TDI, TDO, TCK and the $\overline{\text{TRST}}$ pin. There is no external circuitry necessary excepting a pull down (for example 10 kOhm) at $\overline{\text{TRST}}$.

2.3.4 EJTAG-Interface

The EJTAG interface consists of the EJ_TRST, EJ_TDI, EJ_TDO, EJ_TCK, EJ_TMS the TEST_MODE_EJTAG and the normally not used EJ_BRKIN and EJ_BRK_OUT pins.

In default the TEST_MODE_EJTAG signal must be pulled down to GND with a 10 kOhm resistor or similar. When the EJTAG interface is used the signal must be set high.

When a Lauterbach-Debugger is used you can use the TST-107-01-G.D connector from SAMTEC to prevent a twisted connection to the debugger. There should be ferrite beads in series to the EJ_TDI, EJ_TDO, EJ_TCK, and EJ_TMS signals. You can see an example at the reference schematics.

The EJTAG interface is made to support the developer of the software and to find failures at the board-bringup or reclamations. So the interface is normally not necessary on the board and should not be placed in default.

A cheap and fast available solution is, to provide landing-pads on the PCB which are prepared for an EJTAG/JTAG connector. Such a connector should take the TEST_MODE_EJTAG-pin into account, as this pin is necessary to switch into the EJTAG-mode.



CONFIDENTIAL

Schematic Design Guide

2.4 Reset Circuitry

The INCA-IP2 can be put into reset by the POR reset pin or the HRST reset pin. Only the POR reset pin resets the PLL and latches the pin-strapping signals in. So you should only use the POR signal to start the system.

The HRST reset pin is also a reset output which can be used to hold the peripherals in reset.

You can activate the HRST via software, but if you do this the INCA-IP2 resets itself. So if you need a reset, which is sometimes active in the application, you should use a General Purpose pin.

To make a proper design the following approach is suggested:

- Use only the POR signal as reset input.
- Use the HRST pin or a General Purpose pin as a reset output to hold the periphery in reset.
- There must be a pull-up at the HRST pin, as it is an open drain output. Even if there is nothing else connected to HRST the pull-up is needed, as the HRST is also an input.

The INCA-IP2 has an Under Voltage Protection (UVD). This can be used to hold the INCA-IP2 in Reset until the power is stable. In **Figure 3** you can see a circuitry which delays the system for more than 12 ms. If longer delays are needed because of the periphery of the INCA-IP2, than an external reset device should be used.

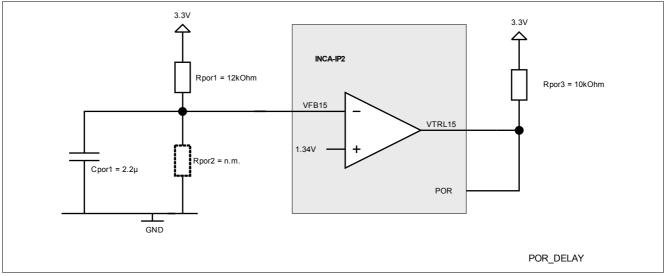


Figure 3 Circuitry to Delay Power On Reset

2.5 Connection to Flash

In all phones there must be a non volatile memory to store the boot-code the operating system and so on.

2.5.1 NOR-Based Flash

The NOR-Based Flash must be connected with CS0 if you want to boot from it. It may irritate that there is a pulldown at CS0 necessary, because of boot-strapping, but pay attention that CS0 is multiplexed with PCI_MOD_SEL0.

The NOR-based flash must be ready before the INCA-IP2 tries its first access. So the reset input of the flash should not be connected to the HRST output of the INCA-IP2, but to the POR input or directly to 3.3 V if the flash is good for that.

2.5.2 NAND-Based Flash

The INCA-IP2 Reference-System gives an example how to connect a NAND-Based flash. ST-Microelectronics recommends to write protect the flash during power-up. This is realized with the HRST output of the INCA-IP2.



Schematic Design Guide

2.5.3 SPI-Flash

The SPI-Flash must be connected to SPI0 interface if you want to boot from it. There must be a pull down at the MRST-pin of the SPI0-interface. Otherwise a boot-up is not possible. Use SSC0_CS0 to connect the SPI-Flash.

2.6 Volatile Memory

As shown in **Figure 4** the INCA-IP2 supports up to four SDRAM modules. In most applications there is only one module needed. For example the phone application for the INCA-IP2 fits with less than 16 MByte easily in a quarter of one module.

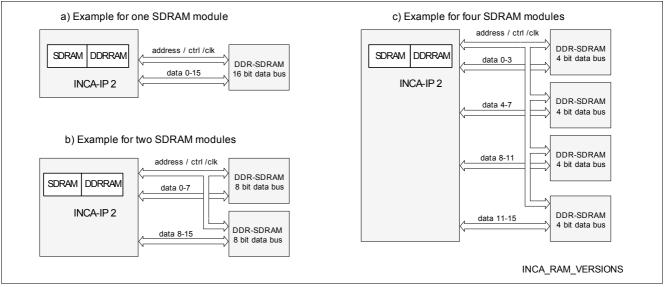


Figure 4 How to Connect SDRAM-Modules

2.6.1 Connection to SDR-SDRAM

There are no special recommendations aside of the normal rules to connect an SDR-SDRAM. Place the RAM close to the INCA-IP2. Series resistors in the data and address-path may help, but are not demanded. Use a 33 Ohm resistor for the CLK, RAS, CAS, WE, DQM0 and DQM1 signal.

2.6.2 Connection to DDR-SDRAM

You can find an example for a DDR-SDRAM interface in the Schematics for the Reference System. This is designed according to **Figure 4** example a). If you need more than one DDR-SDRAM module, you need for each Vref pin a resistor circuitry, but only one termination for SDI_CLK/SDI_CLKN.

In many DDR-SDRAM designs you find an additional termination against a generated mid-voltage, called VTT. You could use this too, but it increases costs, efforts and power-consumption. Such a termination is not necessary.

2.7 Ethernet Interface

2.7.1 Gigabit Ethernet

In dependence of the used external Phy it can be possible to use a 2.5 V device directly to the RGMII interface of the INCA-IP2.

The driver of the RGMII-interface can easily generate noise. Therefore there should be 33 Ohm resistors in series. The TXC0 and TXC1 clock signals should have 68 Ohms in series. You may precautionary place pads for a



capacitor (in the range of some pico farads) directly at the two CLK-pins. If resistor-arrays are used, combine only function groups for each phy. Small packages are preferred, as they allow a narrow placing of the phy. Each of the power-balls at the RGMII should have at least one blocking capacitor. It may be helpful to plan some not placed capacitors.

In the MDIO interface there should be 33 Ohm too.

2.7.2 Internal 10/100-Phys

If the internal Phys are used, the signals RXC0 and RXC1 of the RGMII-Interface must have a pull-up (10kOhms are allowed for example). If this signals are not set to high, the Phys do not work reliable. If an external phy is used, no-pull ups are needed.

In Figure 5 you can see the proposed circuitry for the internal Phy.

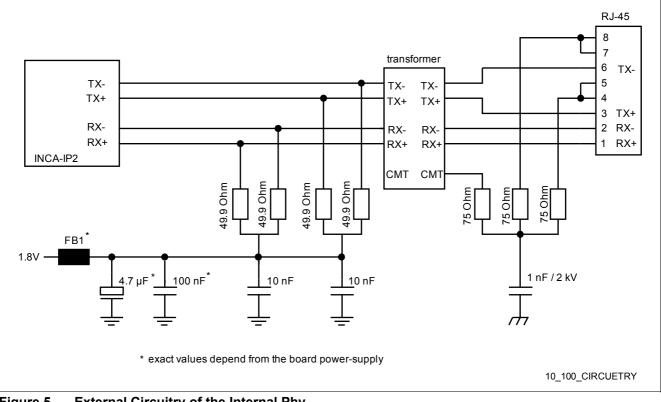


Figure 5 External Circuitry of the Internal Phy

You can find detailed information for the choice of the transformer in chapter 14.4.2 of the User's Manual Hardware Description.

The Inca-IP2 provides a regulator for 1.5 V and 1.8 V for the voltages of the Phy. This voltages can be generated and used for the Phy, but they needn't. The Phy uses the 1.5 V for analogue purposes, so ripple should be minimized.

2.8 ASC0 Terminal Interface

The TXD0 and the RXD0 pads are located very near by the RGMII-Interface. As a result the noise-Influences of this interface are big. While the RGMII-Interface is short, the terminal-interface is often very long. To reduce EMI-influences there should be a 47 pF capacitor against GND on the TXD0 and RXD0-pin. Moreover a series resistor or series ferrite should be placed for this signals.



2.9 Analogue Frontend

2.9.1 Circuitry for Microphones

In **Figure 6** you can see the electronic devices which can be used for connecting the microphone. The basic circuitry shown in sector b) consists of the filter and decoupling filters Cafe4, Cafe5 and Cafe6, and some components to provide the bias-voltage. The components for the bias-voltage may change in dependence of the used microphone and needed quality. Especially the capacitor Cafe3 is designed with much reserve.

In **Figure 6** you can also see an EMI and an ESD-protection in sector c) and d). The INCA-IP2 ESD firmness is tested according to the HBM with 2 kV. According to the target marked and the supported standards you can add the ESD and EMI protection.

In sector a) there is an additional circuitry, which is made to prevent the influence from one microphone to another one. If the circuitry a) is not added, it might happen that loud noise which is detected with one microphone is audible on another microphone. The capacitor Cafe1 should be placed, if there is only one resistor bridge like Rafe1 and Rafe2 for all microphones. You can find more details in Chapter 10.1 from the User's Manual Hardware Description.

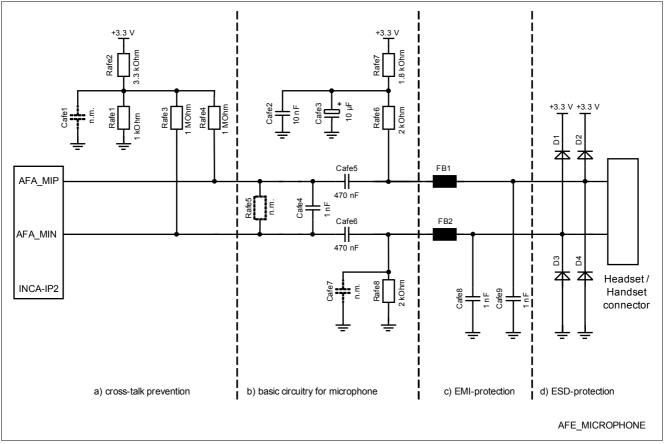


Figure 6 Microphone Circuitry for INCA-IP2

2.9.2 Circuitry for Earpiece Output

In **Figure 7** you can see a connection to the loudspeaker. For fall-back purposes you can place the not mounted capacitors Cafe11, Cafe12, Cafe13.

In case of having a Headset connected to the interface, you can use a headset-detection. This headset-detection recognized if someone plugs or removes the headset. The circuitry can be used, but needn't. The capacitors



Cafe13 and Cafe14 are designed to pass frequencies down to 200 Hz. If smaller frequencies are needed this capacitors must be bigger. In case of using no headset detection no decoupling capacitors (here Cafe13 and Cafe14) are needed.

In **Figure 6** and **Figure 7** there are no names of INCA-IP2 pins used, as the circuitries are valid for all microphones or earpiece outputs.

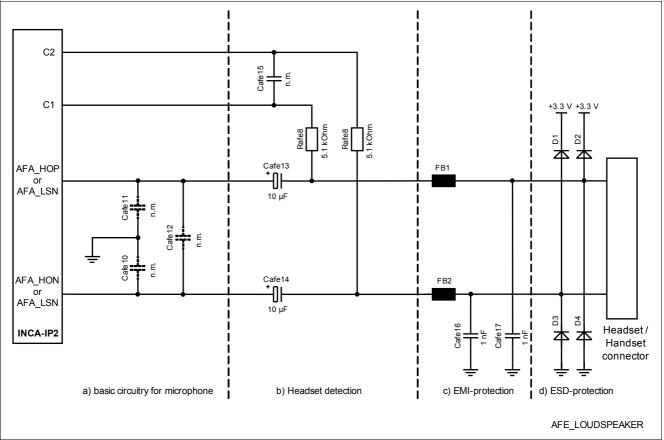


Figure 7 Loudspeaker Circuitry of the INCA-IP2

2.9.3 Circuitries for Loudspeaker

The LSP1/LSN1 signals can be connected directly to a loudspeaker or an external amplifier. The LSP/LSN2 signals must be connected to an external amplifier if they are used, as the INCA-IP2 has no internal amplifier on LSP2/LSN2.

2.10 Circuitry for Keypad

The keypad scanner can work in Standard Matrix Mode and Full Matrix Mode. In Standard Matrix Mode the simultaneous use of each key-combinations is possible, while in Full Matrix Mode more keys can be supported with less key-signals. It is more future-proof to use the Full Matrix Mode.

In **Figure 8** you can see an example for a Full Matrix Mode keyboard. You can see that up to 55 keys can be controlled with only ten key-pins.

This matrix works fine and can detect more than one key at the same time, but the connected signals to each simultaneously used key must not be connected to another pressed key. For example it is allowed to press the "Mailbox"-key and the "Submit"-key at the same time. But it is not allowed to use the "Mailbox"-key and the "Record"-key simultaneously. In this case both keys would use the KEY8-signal.



CONFIDENTIAL

Schematic Design Guide

In the shown example in Figure 8 there is the "Hook" switch realized via keymatrix. If it is carried out this way it would not be possible to activate Hook and press a function key F3 to F12.

The Full Matrix mode is normally used, as it reduces the needed keys and so interfaces are free for later used applications.

Attention: All key-signals which are used for the keyboard must have a pull-up of 20 kOhm or similar.

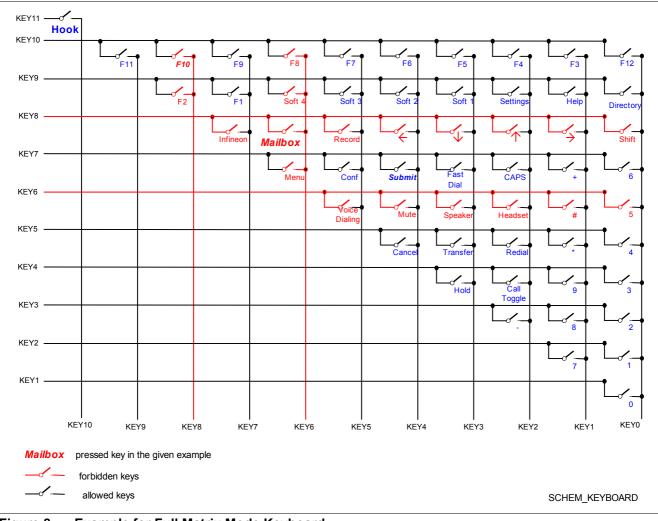


Figure 8 **Example for Full Matrix Mode Keyboard**

2.11 LED-Circuitries

In addition to the extensive descriptions in Chapter 25.2 of the User's Manual Hardware Description the following Annotations may help:

The use of transistors for the LED-matrix is not mandatory. In Figure 9 b) you can see an alternative circuitry without transistors. The limitation of the LED-current (11 mA) is calculated for a lifetime of 100.000 hours. This is far beyond the live-time of LEDs. The live-time of the LED-Pads is reduced to the half, if you double the current.

If you use blue or white LED with high brightness it can bring better results if you use a circuitry like Figure 9 c).

If you want to control the LED of a display with a PWM-signal of the INCA-IP2, than an example is given in the INCA-IP2 reference system. Here the consideration of the correct pin-strapping is needed. The lifetime of backlight LEDs is limited. So it may be needed to reduce the default brightness to achieve the needed lifespan.

If much more than 24 LEDs are needed, this can be realized with shift registers.



Schematic Design Guide

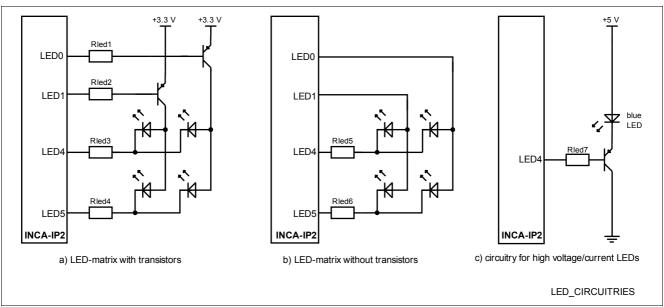


Figure 9 Circuitries for LED-connections

2.12 Checklist for Schematic Release

- Are the date name and the version of the schematics correct?
- Are all nets connected?
- · Are all power-planes connected to a power-supply?
- Are all intentionally not connected pins marked?
- · Are all placing options marked clearly?
- Are there all necessary annotations for the Layouter (for example: differential routing; execution of planes; noise sensitive signals; high voltage areas)?
- Are the function groups drawn obviously, so that the Layouter places the devices correctly?
- Are necessary placing annotations made?
- · Are tolerances mentioned at the devices if there are special needs?
- Are all ten boot-strap signals set correctly according to Chapter 2.1 and do they really meet their voltages in spite of EMI-protections or other external circuitries like PWM-supplements and so on?
- · Are the demanded RESET-durations for each used device fulfilled?
- · Are the demanded jitter-limitations for all devices fulfilled?
- Is the power-on-sequence correct for all devices?
- Is the power-off-sequence correct for all devices? The INCA-IP2 has no requirements for this, but maybe an other devices.
- · Is a need of galvanic separations taken into account?
- Are the outputs connected correctly to inputs, or do misleading pin-names lead to failures (especially at the ASC, SPI and PCM-interfaces)?
- Is a pull-up resistor for all open-drain outputs implemented?
- Is a pull-down resistor for all open-collector outputs implemented?
- Are series resistors at critical signals?
- · Are there any not placed terminations to be on the safe side?
- · Are shared interrupts connected correctly, or may push/pull-driver work against each other?
- · Are all pull-resistors or pin-strap resistors connected to the power-domain of the internal circuitry of the chip?
- · Do the levels of the chip-interfaces meet the requirements of the connected counterpart?
- Is a 68 nF capacitor placed at the BGREF pin of the INCA-IP2?



CONFIDENTIAL

Schematic Design Guide

- If you use the VFB15-ball to generate 1.5 V: Is the requested 2.2 kOhm resistor placed according to the Users Manual Hardware Description?
- Is the JTAG-chain connected correctly and is the EJTAG available for test purposes?
- Are there any spare-pins at the connectors? Spare-pins are often necessary for later improvements and pathes.
- Does the connector fit to the mechanical model?
- Are GND/VCC placed at the connectors in a helpful way do reduce crosstalk and EMI?
- Is the number of various used devices (especially resistors and capacitors) reduced to the minimum to ease logistics?
- Do all devices bear the heat, or are special packages or cooling areas needed?
- Do all external Phys have a different address?
- Are protections implemented (for example over-power-protection for USB or EMI-protections)?



3 Layout

3.1 General Layout-Hints

The INCA-IP2 is a high performance microcontroller which works at high frequencies. Microcontrollers in general need high peak-current while the average current is much smaller. Those high peak-currents can cause significant EMI problems. The unintentionally generated magnetic fields are proportional to the area which is cycled by the current. It is easy to reduce the high peak-currents by using block capacitors. If this capacitors are placed correctly at the area of the loop for the peak current is small. As a result the unintended magnetic fields are small. You can see this in **Figure 10** a) and b).

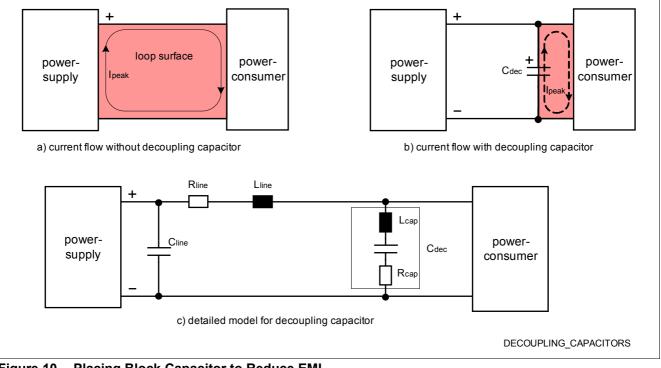


Figure 10 Placing Block Capacitor to Reduce EMI

High speed ICs like the INCA-IP2 operate in frequency bands where passive components can not be considered as ideal any more. A more detailed model is shown in **Figure 10** c). As a result of the parasitic inductances and resistances, a part of the peak-current is not provided by the block capacitors. The higher Rcap and Lcap are, the more current is provided via Rline and Lline.

Aside of the power-consumption the data-signals can be reasons for EMI. If the signals are routed via GND-plane or the according power-plane the unintended magnetic fields are small.

This are the conclusions for a good Layout:

- The block capacitors must be placed as near by the consumer as possible.
- The current should pass the block capacitors if possible.
- If a double sided placement is made the placing of the block-capacitors should be under the BGA.
- · Use small packages preferred, as they have less parasitic inductances and resistances.
- · Place the components near by each other to avoid long antennas
- If a six-layer-design is used, the aggressive signals should be routed in the inner layer.

Aggressive signals are characterized by its driver and the number of level-changes. A strong driver causes a fast level-change. According to Fourier analysis higher frequencies are used. If those fast level-changes are not



needed, the use of series resistors or capacitors against GND can reduce it. The most aggressive signals of the INCA-IP2 are the RGMII-signals (especially TXC0 and TXC1) and the SDRAM-Interface signals.

The positive effect of a GND-plane is strongly dependent of its design. Unintended separations are often a reason for significant EMI.

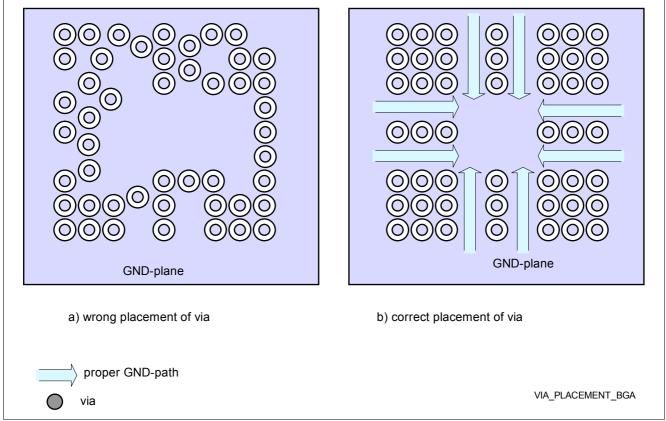


Figure 11 Arrangement of Vias under a BGA

In **Figure 11** a) you can see a typical BGA-layout which often leads to significant problems. In general the GNDplane is connected, but there is no big path with low inductance. There is also no good conductivity for heat. In **Figure 11** b) you can see an arrangement with the same number of vias, which is much better. In the layout studies of **Chapter 4** you can see an example for the INCA-IP2.

Another reason for unintended separations of planes is shown in **Figure 12**. Here the simultaneous layer-change of a signal group can cause separations. A simple shift of the vias can solve this issue.



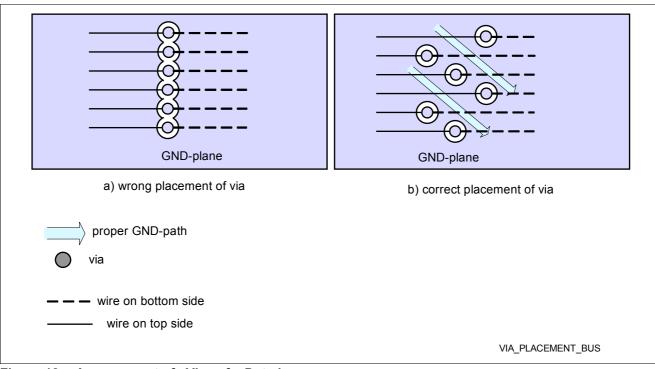


Figure 12 Arrangement of vVias of a Data-bus

3.2 Execution of the GND-Plane

You can find three GND-areas on the board. First the Area for Power of the Ethernet-connection, Second the Power over Ethernet GND and last but not least the general GND of the other Board Power Supplies. The first two areas should be limited to the according areas whereas the general GND should cover the rest of the Board. The general GND should be as solid as possible. Avoid unintended separations by vias or wires.

The free spaces on the top and bottom-side can be filled with GND. This GND-areas must be connected to the GND-Plane very well with vias. Open Ends of such GND-areas need to be connected urgently to the GND-plane.

In the middle of the INCA-IP2 there are many GND-pins. This is not only good for the power-consumption, but also helps to spread the heat and reduces EMI. A good connection to the GND-Plane with several vias mandatory for this.

To improve the GND-connection of the INCA-IP2 you can provide a small plane directly on the placing side of the INCA. This plane can include the pins TEST_CLK1, TEST_CLK2, TEST_CLK3, TEST_CLK3 and TEST_MODE_CLK.

This Plane can be connected to other GND-Areas on the placing side via two pathes. One is possible via the pins H1 to H7 and the second path can be made via E15 to E18 if a crystal is used and the OBYP-pin is strapped directly to GND.

3.3 Execution of the Power-Plane

The power-planes should serve as a reference-plane for the signals. The 2.5 V DDR-SDRAM signals should refer to the GND or 2.5 V plane and the other signals of the INCA-IP2 should refer to the 3.3 V plane. In **Figure 13** you can get an idea of a possible power-plane.



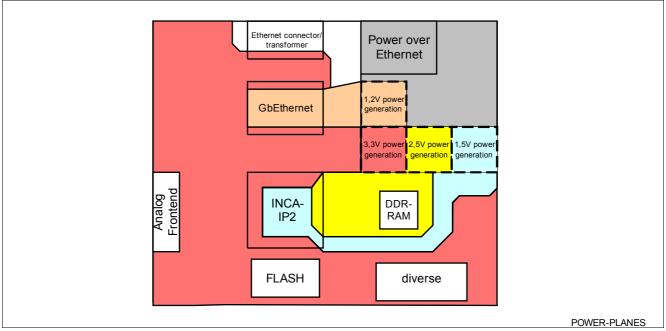


Figure 13 Ideas for Power-planes

3.4 Layer Stack Setup

The INCA-IP2 is designed for a four-layer design. In case of using an external phy, the use of six layers can be helpful to achieve good Electromagnetic Compatibility (EMC). The signal-layer and GND/power-layer must be symmetrical. Aside of that no recommendations are given. If no impedance matching is needed for a bus like the RGMII or the External Bus Unit (EBU), there should always be a plane as a reference.

3.5 Layout of the Crystal or Oscillator

Place the crystal close to the INCA-IP2 but keep aggressive signals away. This means that the RGMII-signals or the internal Phy-signals should not be routed to near to the Crystal.

The spreads area which is generated by the signals to XTAL1 and XTAL2 should be as small as possible.

If an oscillator is used, this should also be as near to the INCA-IP2 as possible.

The power-filter for the Crystal-circuitry of the INCA-IP2 should also be as near to the INCA-IP2 as possible.

A special preparation (shown in **Figure 14**) of the GND-plane is getting more popular and leaded to good results at related products of the INCA-IP2.



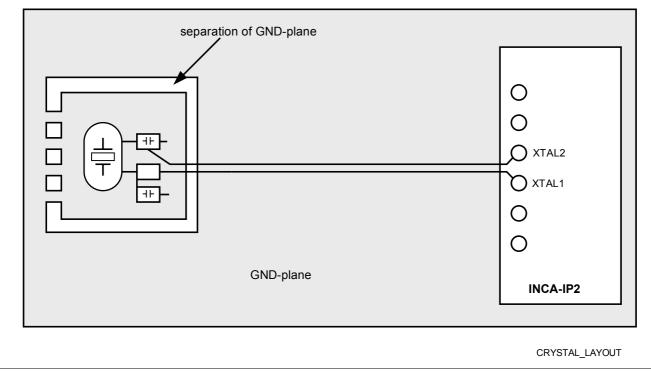


Figure 14 Layout of Crystal

3.6 SDR-SDRAM Layout

A length matching of +/- 250mil of all lines related to the CLK of the SDR-SDRAM should be achieved. The blocking capacitors should be placed carefully.

3.7 DDR-SDRAM

A layout-failure at the DDR-SDRAM module can make the board useless, even for the first bring up. Consequently special attention is needed here. It is worth of it to plan at least four design-days for the DDR-SDRAM layout.

There are three major issues which can reduce the signal integrity. First there are reflections on the lines. Second there is the cross talk and the most important issue is the unequal signal propagation.

3.7.1 Layout Rules against Reflections

The series resistors in the lines are a sufficient protection against reflections. It is not important if they are placed near by the INCA-IP2 or the DDR-SDRAM devices.

The resistor circuitry for the CLK lines should be placed at the DDR-SDRAM device, if one is used, or at the branch of the signals, if several DDR-SDRAM chips are used.

3.7.2 Layout Rules against Cross Talk

The cross talk is easy to overcome if the following recommendation are taken into account:

- The signals should be routed in groups which use the same planes. It is allowed to use the 2.5 V and the GND for reference. There are three groups: Data-Lines (SDI_DQ0-15, SDI_DQS0-1; SDI_DM0-1), Address/Command/Control-Lines (SDI_A0-13, SDI_CAS, SDI_RAS, SDI_WE, SDI_CKE, SDI_CS) and clocks (SDI_CK, SDI_CKN).
- The minimum distance to other signals of the group is 15 mil (0.13 mm)
- The distance to signals of other signal groups is at least 30 mils (0.74 mm)



• Serpentine isolation spacing must have 20 mils (0.5 mm) at least.

3.7.3 Layout Rules against unequal Signal Propagation

At this synchronous interface the data is latched with an edge. This falling or rising edge must fit to the rest of the data. Especially the data-line is sensitive, as it works with the double data-rate. To ensure a secure data-transfer the load and the distance of the signals must be under restrictions.

The following rules must be taken into account:

- The maximum difference in data lane to data strobe length is +/-25 mils (0.625 mm). SDI_DQ0-7 must meet SDI_DQS0 and SDI_DQ8-15 must meet SDI_DQS1.
- When more than one clock pair is used (when using two or four chips) the clock-pair-to-clock-pair must match within 20 mils
- The clock-length must be in the middle of all data-length.
- The Address/Command/Control-Lines must not differ more than +/- 200 mil (5 mm) to the SDI_CLK/SDI_CLK signals.

If more than one DDR-SDRAM is used the trace length from each data-group (8*DQ+DQS+DM) controller bond pad to the data-pad must match to 100 mils (2.54 mm) and the trace length to +/- 100 mils (2.54 mm) across the entire channel.

While routing the signals, the length of the vias and the internal bond length must be taken into account.

DDR_RAM_Signal		
SDI_A0	4679,22	184,221
SDI_A1	5706,46	224,664
SDI_A2	4612,54	181,596
SDI_A3	6367,04	250,671
SDI_A4	5269,67	207,467
SDI_A5	5551,52	218,564
SDI_A6	4925,34	193,911
SDI_A7	6281,84	247,317
SDI_A8	5169,71	203.532
SDI_A9	6782,62	267,032
SDI_A10	7925,36	312,022
SDI_A11	5716,66	225,065
SDI_A12	4103,11	161,540
SDI_A13	4588,09	180,633
SDI_DQ0	5934,16	233,628
SDI_DQ1	4941,43	194,544
SDI_DQ2	5234,81	206,095
SDI_DQ3	4040,01	159,056
SDI_DQ4	5325,29	209,657
SDI_DQ5	5214,13	205,281
SDI_DQ6	4357,55	171,557
SDI_DQ7	4355,48	171,476
SDI_DQ8	5494,58	216,322
SDI_DQ9	5346,26	210,483

Table 2 Internal Length of DDR-SDRAM Signals (BGA-324 Package)



DDR_RAM_Signal		
SDI_DQ10	3969,68	156,287
SDI_DQ11	6151,29	242,177
SDI_DQ12	5898	232,205
SDI_DQ13	4746,23	186,859
SDI_DQ14	4686,46	184,506
SDI_DQ15	4840,2	190,559
SDI_DQS0	5151,03	202,796
SDI_DQS1	6893,12	271,383
SDI_BA0_N	5901,95	232,360
SDI_BA1_N	8279,19	325,952
SDI_CAS_N	4696,02	184,883
SDI_CKE	5618,98	221,220
SDI_CLK	6607,43	260,135
SDI_CLK_N	7967,59	313,685
SDI_CS_N	5501,39	216,590
SDI_DM0_N	8447,6	332,583
SDI_DM1_N	7952,49	313,090
SDI_RAS_N	6903,44	271,789
SDI_WE_N	6380,89	251,216

Table 2 Internal Length of DDR-SDRAM Signals (BGA-324 Package) (cont'd)

3.7.4 Additional Layout Rules

- Place the Vref generation as close as possible to the DDR-SDRAM pin.
- Route all clock pairs on the same critical layer. Avoid switching between layers except where required
- Use of resistor networks for damping resistor is not recommended. If they are used than do not mix signal groups.
- The trace with is usually 5 mil (0.13 mm) and the impedance matching is 60 Ohms.
- The distance between INCA-IP2 and DDR-SDRAM should be as small as possible to reduce EMI. The theoretical length of a wire must not exceed 2.95 inch (75mm).
- Care for proper GND and 2.5 V planes which are not separated because of the use of vias.

3.7.5 Final Annotations to DDR-SDRAM Layout

A layout according the rules above is secure. Often the rules contradict other needs of the board. It is helpful to stay as near to this rules as possible. If you can not follow the rules completely this needn't end in failures. On the Reference-System for example the impedance of the lines is around 70 Ohms.

The DDR-RAM should be as near to the INCA-IP2 as possible, but this makes the layout more difficult. The Reference-System shows a compromise for a four-layer design.



3.8 Layout of the Ethernet Interfaces

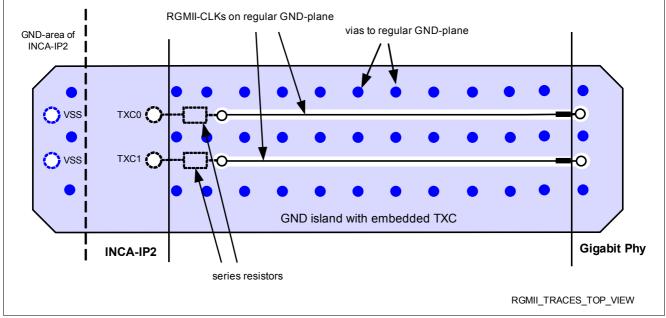
3.8.1 Layout of the Internal Phy

You can find detailed hints for the Phy-Layout in the User's Manual Hardware Description chapter 14.5

3.8.2 Layout of external Phys

The RGMII is a significant noise source. As a result it should be routed very carefully. Normally the function of the phone is not affected, but intended certifications are endangered.

In case of the INCA-IP2 a layout-weakness reasoned by to strong CLK-signals is known. The TXC0 and TXC1 must be routed carefully and shielded. They must not be routed on the top or bottom-layer. In **Figure 15** and **Figure 16** there is an example for a shielded routing. The CLKs are routed inside the GND-plane and below and above the CLKs there are also GND-planes. To achieve a good connection between the planes, many vias have to be placed.





In **Figure 16** you can see the elevation of the PCB. For a perfect layout the distance a) and distance b) should be small, to be a good reference for the CLK-signals (distances of 200 μ m (~8 mil) are typical). In the shown example the regular GND-plane is used to route the signals, but in general also the VCC-plane could be a solution. In case of using the regular GND-plane you must ensure that the distance to the external Phy is small to reduce the GND-separation. The path for other currents should not be interrupted. In case of using the VCC-plane for the CLK-signals it is also needed to have a continuous GND reference for the CLK-signals.

The series resistors mentioned in **Figure 16** can have a value between 68 Ohms and 100 Ohms. 68 Ohms is the calculated value to remove overshoots on the signals.

It is not necessary to route the transmit signals of the RGMII of the INCA-IP2 in a shielded way.



Layout

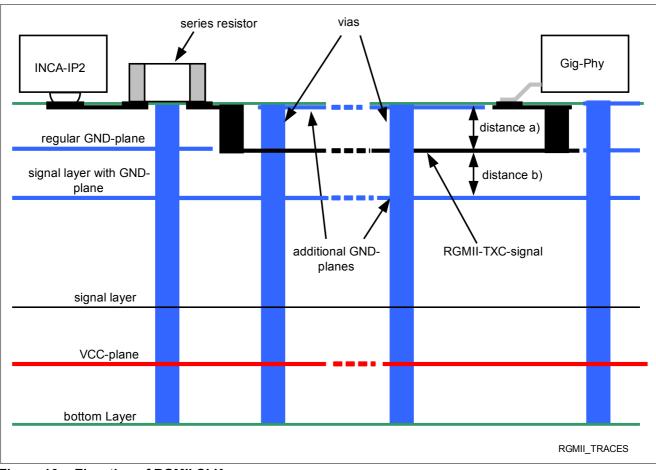


Figure 16 Elevation of RGMII CLKs

For a successful layout the final hints will help:

- Place the series resistors of the transmit path and the CLKs very near to the INCA-IP2.
- Route the signals in function-groups with a GND-plane only. This reference-plane must not have significant damages and must be adjacent directly.
- Place the phy as near to the INCA-IP2 as possible, but care that this does not lead to a damage of the GNDplane.
- The external Phy should have its own crystal or oscillator (at least as a placing option).
- The analogue part should be routed according the layout rules of the Phy. Special care is needed, if there is a common clock-source for INCA-IP2 and the external Phy.

3.9 Layout of the AFE

In **Figure 6** and **Figure 7** you can see the circuitries for the Analog Frontend. EMI-Protection as well as the ESDprotection should be placed as near as possible to the connected cables. The decoupling capacitors Cafe5 and Cafe6 of **Figure 6** of the microphone should be placed near by the INCA-IP2. The filter for the bias-voltage (Rafe6/Rafe7 and Rafe8) should be near by the connected cable.

The following rules should be followed:

- The loudspeaker signals as well as the microphone-signals (HOP/HON, LSP/LSN, MIP/MIN) must be routed differential. This is very important.
- Route the loudspeaker signals as well as the microphone signals via a solid GND-plane. The use of the 3.3 V-plane is allowed, too.
- The Layout of the microphones has priority above the loudspeaker layout.



- Avoid long tracks to the microphone and the loudspeaker.
- The microphone signals as well as the loudspeaker signals which go to an external amplifier should be routed carefully to prevent crosstalk. Do not route this signals in parallel with digital signals.
- Strive for a pair to pair distance, which is four times bigger than the signal to signal distance. A valid example would be if the MIP/MIN signals have a distance of 10 mil (0.25 mm) and the distance between HOP/HON is 50 mil (1.27 mm).
- Avoid multiple Vias in the path of the Analogue Frontend.
- A special impedance matching is not needed.

3.10 Layout of ASC0

The pads of the ASC0 can be victims of EMI-influences of the RGMII-Interface. As a result the prepared EMIprotections should be placed near by the INCA-IP2.

3.11 USB-Layout

- A continuous GND is needed below the DP_USB/DN_USB signals
- Maintain close to 90 Ohms differential impedance. Trace with and spacing needs to be calculating according to the PCB-characteristics.
- The trace must be big enough for the needed currents.
- Maintain symmetry between DP_USB and DM_USB in regards to shape. Trace lengths should be matched.
- Keep unrelated signal traces, supplies and components 5 times the trace width or 35 mils away from DP_USB/DM_USB traces.

3.12 Hints to be realized in Software

Use the slowest needed clock frequency to reduce EMI.

Use the weakest working driver, if a device offers more than one strength.

3.13 Checklist for Layout-Release

If you can agree to all these questions below, you may have a good layout:

- Is the inscription updated to the most resent version?
- Does the schematic developer agree to the placement?
- Is the GND-Plane proper and are the vias placed in a way which does not separate the plane?
- Are all wires big enough for the current (especially PoE-lines from RJ45-connector and the 5 V-Supply and USB)?
- Are all power-supplies routed according the layout-rules of the supplier?
- Are no additional capacitors necessary, as the layout is unforeseen for the schematic developer? Sometimes the mechanical situation makes additional components necessary.
- Is no improvement of the Layout possible, as the order of signals in the Schematics is perfect (especially at connectors)? Often the layout is easier and better when pins are switched on a bus, or other General Purpose pins are used.
- Are there no misunderstandings at the connectors? Is there no unintended twist in the signal-order because of a different mechanical orientation or material change?
- Is the power-connector connected to the plane with a sufficient number of vias?
- Is the copper-distribution on the plane made in a steady way which prevents a deformation caused by temperature?
- · Is the layer-stack symmetrical to avoid mechanical problems?
- Are thermal pads of power-generations, phys and so on connected correctly to the according planes?
- Does the placing of big power-consumer fit to the housing in terms of heat generation?



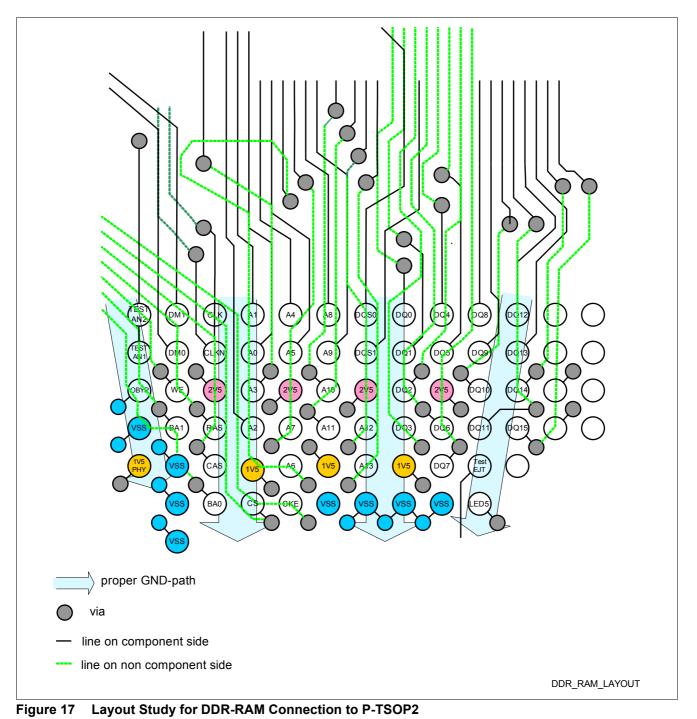
- Are there no aggressive signals routed in parallel to Interrupt signals which could cause unintended interrupts?
- Are there no aggressive signals routed in parallel to Reset signals which could cause unintended resets?
- Are all block capacitors placed at the intended chips and does the current pass the capacitors?
- Are series resisters preferred placed near by the source (especially at clocks)?
- Are digital and analogue signals routed perpendicular if they have to cross each other and are those signals separated with planes?
- · Are all MIP/MIN signals routed in parallel and over GND/VCC?
- Is parallel routing of analog and digital signals avoided?
- Are right angles in signal-layout avoided? Right angles can cause reflections.
- Is the number of vias for signals reduced?
- Are all GND-mini-planes connected with vias. Are there really no open GND-ends which should be connected to the GND-plane?



Layout Study

4 Layout Study

This layout study is made to ensure the feasibility of a four-layer design with the INCA-IP2 (BGA324 package). The scales are not adjusted. The layout study is made width the assumption that the maximum width of the lines is 0.13 mm (5 mil). The names in Figure 17, Figure 18 and Figure 19 are shortened sometimes.



In **Figure 17** you can find the study for a connection to a DDR-SDRAM interface of a TSOP-2. The vias under the INCA-IP2 are placed very carefully with the intention to damage the GND and 2.5 V plane as little as possible. This is important for a good Electromagnetic Compatibility (EMC). The light blue arrows show pathes which allow the current to return easily. If a six-layer Printed Circuit Board (PCB) is used, the arrangement of the vias allows a perfect placing of blocking capacitors under the INCA-IP2.



Layout Study

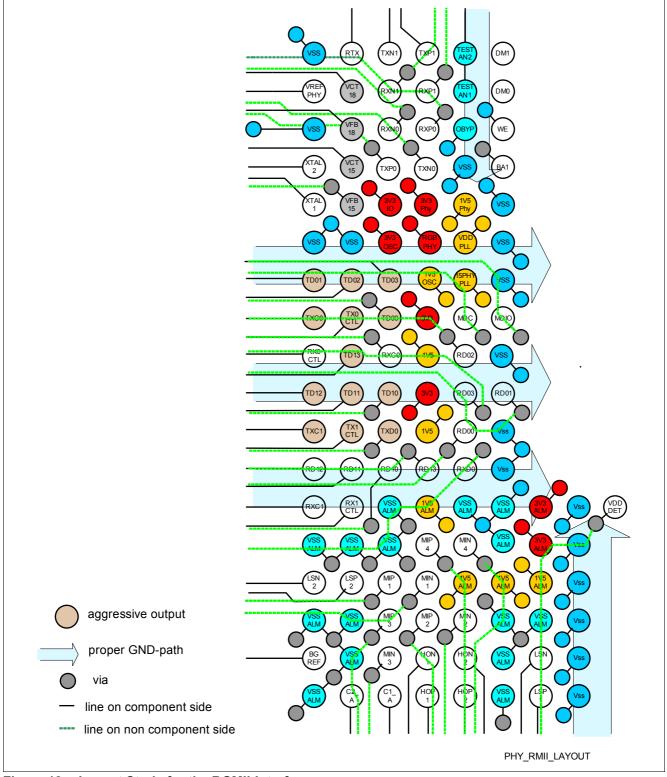


Figure 18 Layout Study for the RGMII-Interface

The RGMII-Interface shown in **Figure 18** can easily generate significant noise. The strongest used pad-driver are used for the TXC0 and TXC1 pads. This lines should be referenced perfectly to a plane.



Layout Study

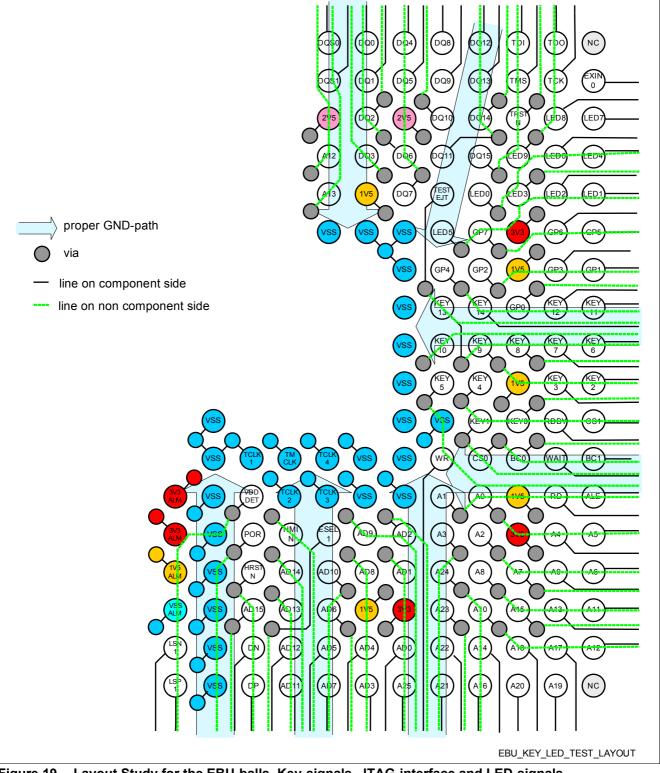


Figure 19 Layout Study for the EBU-balls, Key-signals, JTAG-interface and LED-signals

The final layout for the shown interfaces in **Figure 19** will differ for each application. According to the used pinmultiplexing the layouter may prefer special signals. If VDDDET is set directly to GND this improves one GNDpath.



Terminology

Terminology

A AFE ALE	Analogue Front End Address Latch Enable
D SDR-SDRAM DDR-SDRAM DCL	Single Data Rate Synchronous Dynamic Random Access Memory Double Data Rate Synchronous Dynamic Random Access Memory Data Clock
E EBU EMI ESR	External Bus Unit Electromagnetic Interferrence Equivalent Series Resistance
F FSC	Frame Synchronizer
G GbE GND	Gigabit Ethernet Ground Potential
H HBM	Human Body Model
I INCA-IP2 I/O	Infineon Single Chip Solution for IP Phone Application Input/Output
L LAN	Local Area Network
M MELF μC	Metal Electrode Face (Discrete Leadless Component) Microcontroller
PC PCB ppm	Personal Computer Printed Circuit Board Parts per million



Terminology

R	
Rx	Receive Direction
S	
SOC	UTOPIA Signal–Start Of Cell
т	
Тх	Transmit Direction

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